30 GHz Multi-Bit Monolithic Phase Shifters*

by

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Abstract

The design and performance of GaAs monolithic 3-bit and 4/5 bit switched line phase shifters for Ka-band operation are discussed. Both conventional recessed and self-aligned gate (SAG) switching FET designs are presented. The insertionloss was as low as 2dB per bit for the recessed gate and 2.9 dB per bit with the SAG gate devices for the particular doping levels used.

I. INTRODUCTION

The electronically steered antenna is a key component in the overall development of a solid state active array for communications and radar systems. An integral part of such an antenna is the phase shifter used to control the direction of the beam. The size and cost of conventional multi-bit phase shifters is a problem at Ka-band which monolithic designs can potentially solve. This paper discusses 3-bit and 4/5-bit monolithic phase shifters with a demonstrated insertion loss as low as 2 dB per bit near 30 GHz. These are believed to be the first multi-bit monolithic phase shifters demonstrated at Ka-band.

II. DESIGN APPROACH

Switched microstrip line designs are used for the 45, 90 and 180 degree phase shifter bits. The differential lengths between alternate signal paths is used to control the phase shift. This design results in true time delay and maximum bandwidth for an array antenna. Power consumption and loss are reduced by using low resistance, 400 micron, unbiased FETs [1-4] for switching the signal paths. They are connected in series with the switched lines to reduce the size of the circuit and to eliminate the need for forming vias through the substrate.

The 22.5 and 11 degree increments are implemented using a loaded transmission line. The phase shift is continuously adjustable by controlling the bias of FETs connecting short capacitive stubs to the main transmission line.

Two different layouts were employed for the 4/5 bit phase shifter as shown in Figure 1. The first design uses separate bonding pads for the gate of each switching FET. The second connects the gates of similarly biased FETs together through decoupling networks. Both designs use the same switched transmission line design for the three most significant bits and a loaded transmission line for the final two bits.

The 3-bit phase shifter design was similar to that used for the most significant bits of the 4/5 bit design.

III. FABRICATION METHODS

Two different fabrication procedures were employed for the 3-bit phase shifters: a conventional recessed gate approach and a self-aligned gate (SAG) [4,5] technique. The 4/5 bit phase shifters were fabricated using recessed gate designs. The FET's were produced by direct ion implantation into undoped LEC material and the microstrip lines were formed on the semi-insulating substrate. The "on" resistance of the SAG FETs was about 9-11 ohms while the "on" resistance of the recessed gate devices was as low as 6 ohms. Device design and fabrication techniques required to obtain these resistive parasitics will be presented at the symposium.[4]

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IV. RESULTS

The test fixture for the 4/5-bit phase shifter is shown in Figure 2. A similar design was used for the 3-bit device. It contains two fin line transitions from Ka-band waveguide to microstrip, control input terminals and phase shifter mounting block. The test fixtures contribute 1.1 dB to the measured insertion loss.

The two different fabrication techniques employed for the 3-bit phase shifters gave similar results for the doping levels employed. The measured phase shift vs frequency curves are regularly spaced except for the switch from 135 to 180 degrees. For this case all of the phase bits are changing state and their errors are cumulative.

The minimum insertion loss obtained for the SAG phase shifters was 2.9 dB per bit while the recessed gate devices demonstrated values as low as 2 dB per bit. The difference could be ascribed to the lower doping levels and higher gate metal resistance for the self-aligned gate devices.

A 4/5-bit phase shifter mounted in the test fixture is in Figure 3. The fin line transitions to waveguide are on either side with control inputs at the top and bottom. The phase delays operating as a 4-bit or 5-bit phase shifter are shown in Figures 4 and 5, respectively. The insertion loss for the 4-bit states is given in Figure 6 for frequencies from 27.5 to 30 GHz.

V. SUMMARY

Multi-bit phase shifters have been demonstrated at 30 GHz using both recessed and self-aligned gate techniques. The results achieved show promise for future system applications.

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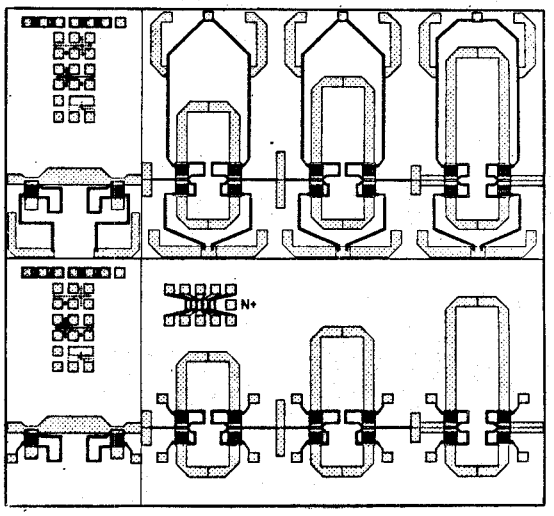

Figure 1. Two versions of the 4/5 Bit Phase Shifter Layout.

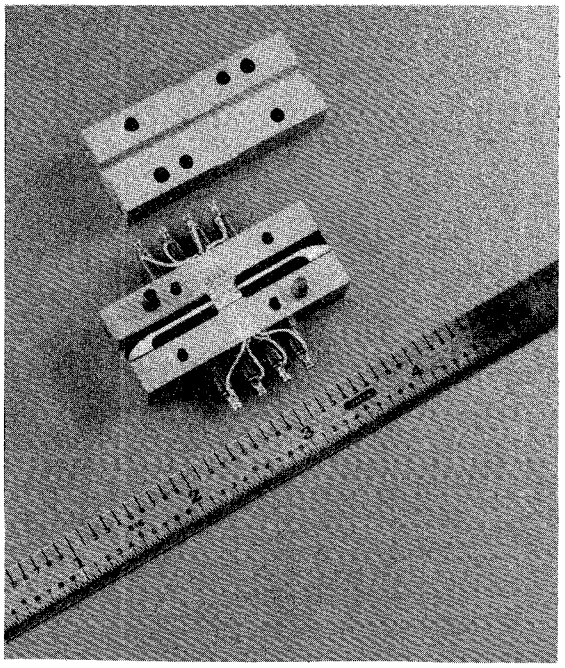

Figure 2. Test Fixture for the 4/5 Bit Phase Shifter.

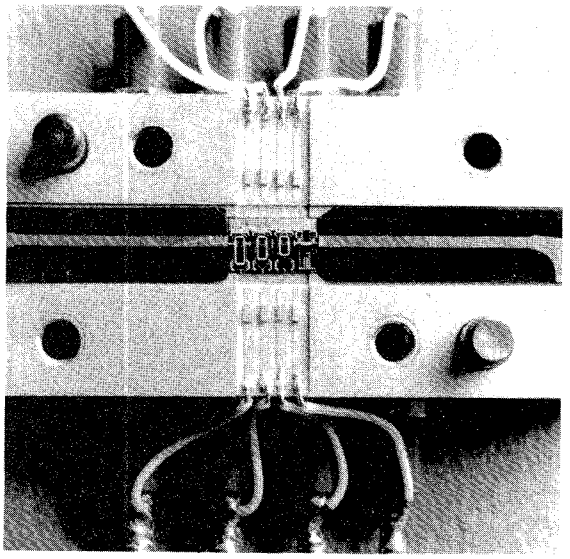

Figure 3. 4/5 Bit Phase Shifter Mounted in Test Fixture.

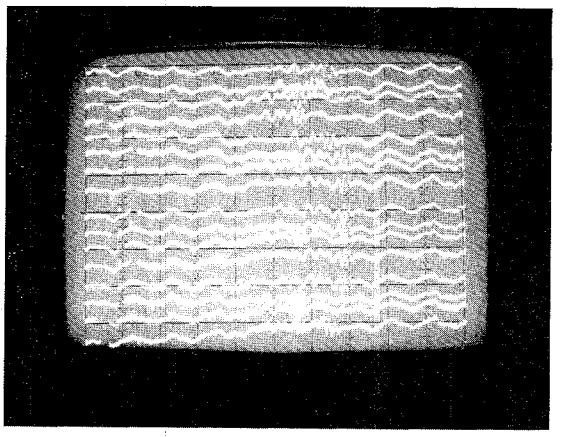

Figure 4. Insertion Phase versus Frequency for 4 Bit Operation of the 4/5 Bit Phase Shifter. Horizontal Range: 27.5 to 30 GHz. Vertical Scale: 45°/div.

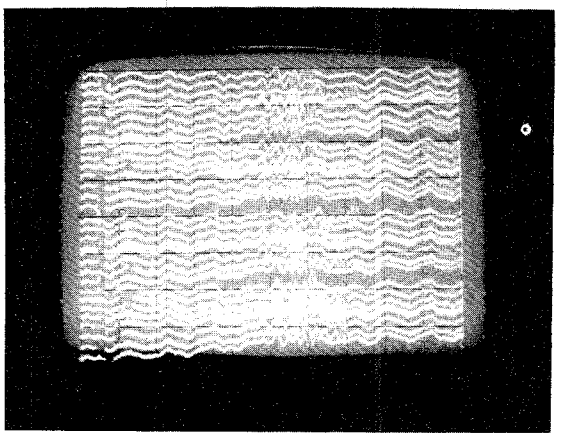

Figure 5. Insertion Phase versus Frequency for 5 Bit Operation of the 4/5 Bit Phase Shifter. Horizontal Range: 27.5 to 30 GHz. Vertical Scale: 45°/div.

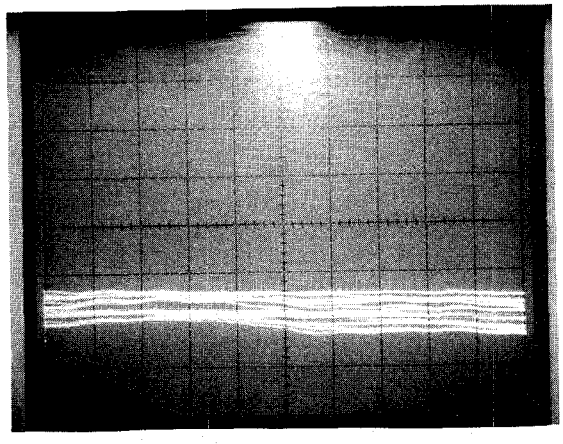

Figure 6. Insertion Loss for 4-Bit Operation of the 4/5 Bit Phase Shifter. Horizontal Range: 27.5 to 30 GHz. Vertical Scale: 5 dB/div (Center Reference.)